REMARKS

The Office Action mailed on February 20, 2003, has been received and reviewed.

Claims 1-22 are currently pending and under consideration in the above-referenced application. Each of claims 1-22 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that an Information Disclosure Statement was filed in the above-referenced application on November 28, 2001, but that an initialed copy of the PTO-1449 that accompanied that Information Disclosure Statement has not yet been returned to the undersigned attorney. It is respectfully requested that the information cited in the Information Disclosure Statement be considered and made of record in the above-referenced application and requested that an initialed copy of the accompanying PTO-1449 evidencing such consideration be returned to the undersigned attorney.

Preliminary Amendment

Also, note that a Preliminary Amendment was filed in the above-referenced application on February 27, 2002, but that entry thereof in the above-referenced application has not yet been acknowledged by the Office. If, for some reason, the Preliminary Amendment has not been entered into the Office file for the above-referenced application, the undersigned attorney will be happy to provide a true copy thereof to the Office.

Drawings

Proposed corrections to FIGs. 6 and 14 of the drawings are respectfully submitted herewith, under separate cover of a Letter to the Chief Draftsman.

The proposed changes include revision of FIG. 6 to add the reference numeral 21 with appropriate lead line and of FIG. 14 to include reference numeral 49, along with its appropriate lead line. The proposed corrections have been marked in red. It is respectfully submitted that neither of these revisions introduces new matter into the above-referenced application.

In addition, corrected formal drawings are submitted herewith under cover of a separate Transmittal of Formal Drawings.

Rejections Under 35 U.S.C. § 102(e)

Claims 1, 2, and 10-22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,146,968 to Lu et al. (hereinafter "Lu").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference that qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Furthermore, the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Additionally, the elements must be arranged as required by the claim, but identity of the terminology is not required. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990).

Lu describes a process for forming the bottom electrode of a storage capacitor of a semiconductor device. The process includes, among other things, forming a capacitor opening 110 through a silicon nitride layer 108 and an underlying oxide layer 106 of a semiconductor device structure. Col. 2, lines 40-46. A rugged polysilicon layer 112 is then formed over the silicon nitride layer 108 and on the surfaces of the capacitor opening 110. Col. 2, lines 47-59. As shown in Figures 3-5 of Lu, the rugged polysilicon layer 112 merely coats the surfaces of the capacitor opening 110; it does not substantially filly the capacitor opening 110. Next, a photoresist layer 114 is formed over the rugged polysilicon layer 112. Col. 2, lines 60-63.

Thereafter, various etching processes are conducted to completely remove the photoresist layer 114 and to remove portions of the rugged polysilicon layer 112 that overlie the silicon nitride layer 108.

Notably, Lu explains, at col. 3, lines 56-58, that use of the process flow described therein eliminates the need for chemical mechanical polishing (CMP), a well-known planarization technique.

Independent claim 1 is drawn to a method for preparing a surface of a semiconductor device structure for planarization. The method of independent claim 1 includes, among other things, providing the semiconductor device structure with a first material layer. The first material layer has a nonplanar surface, covers a surface of the semiconductor device structure, and substantially fills at least one recess in the semiconductor device structure.

Lu lacks any express or inherent description of providing a semiconductor device structure that includes a recess which is substantially filled with material of a first material layer. Rather, as Figures 3-5 of Lu quite clearly depict, the first material layer (*i.e.*, rugged polysilicon layer 112 (Office Action, page 2)) of the illustrated semiconductor device structure merely *coat* the surfaces of each capacitor opening 110; the rugged polysilicon layer 112 does not *substantially fill* the capacitor opening 110.

Accordingly, it is respectfully submitted that Lu does not anticipate each and every element of independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(e). It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 1 is allowable over Lu.

Claims 2 and 10-22 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 2 is additionally allowable because Lu lacks any express or inherent description that the photoresist layer 114 thereof comprises a stress buffer material. As explained at paragraph **[0018]** of the specification of the above-referenced application, a stress buffer material "facilitates planarization . . . without causing substantial defects" in an underlying material layer. Lu lacks any express or inherent description that the photoresist layer 114 thereof facilitates planarization. Further, Lu emphasizes that the process described therein eliminates the need for CMP, a well-known planarization technique. Col. 3, lines 56-58.

Claim 10, which depends from claim 2, is further allowable since Lu does not expressly or inherently describe that the photoresist layer 114 may be spread such that one valley of the underlying rugged polysilicon layer 112 may be at least partially filled while at least one peak of the underlying rugged polysilicon layer 112 may remain substantially uncovered. Rather, Lu clearly describes that, when spread, the photoresist layer 114 covers all of the rugged polysilicon

layer. *See,* Figure 3; col. 2, lines 60-63. In fact, none of the peaks of the rugged polysilicon layer 112 is exposed until the first etching process is conducted. *See* col. 2, line 65, to col. 3, line 3.

Claim 11 depends from claim 10 and is also allowable since Lu neither expressly nor inherently describes that the rugged polysilicon layer 112 thereof may be planarized.

Claim 13, which depends from claims 11 and 12, is additionally allowable since Lu includes no express or inherent description that the rugged polysilicon layer 112 may be etched with selectivity over the photoresist layer 114 thereof *and* until a surface of at least one region of the rugged polysilicon layer 112 is in substantially the same plane as a surface of the photoresist layer 114. Rather, the exposed surfaces of the rugged polysilicon layer 112 and photoresist layer 114 of the semiconductor device structure of Lu are in substantially the same plane *before* selective etching is effected. *See* col. 3, lines 1-25.

Claim 14, which depends from claim 13, is further allowable because Lu does not expressly or inherently describe abrasively planarizing either the photoresist layer 114 or a region of the rugged polysilicon layer 112. Rather, Lu teaches that CMP, a well-known abrasive planarization technique, is not required. Col. 3, lines 56-58.

Claim 21, which also depends from claims 2, 19, and 20, is additionally allowable since Lu neither expressly or inherently describes that the rugged polysilicon layer 112 and the photoresist layer 114 thereof may be concurrently abrasively planarized. Again, Lu teaches that CMP, a well-known abrasive planarization technique, is not needed. Col. 3, lines 56-58

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, and 10-22 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Claims 3-9 stand rejected under 35 U.S.C. § 103(a).

M.P.E.P. 706.02(j) sets forth the standard for a rejection under 35 U.S.C. § 103(a):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation,

> either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Lu in View of Yoshihara

Claims 3-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu in view of U.S. Patent 6,117,486 to Yoshihara et al. (hereinafter "Yoshihara").

Each of claims 3-5 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Moreover, it is respectfully submitted that neither Lu nor Yoshihara, taken either separately or together, teaches or suggests each and every element of claim 3.

Yoshihara teaches a resist coating method that includes applying resist to a substrate as the substrate is being rotated, decreasing the rate of rotation of the substrate for a predetermined period of time, and re-increasing the rate at which the substrate is rotated. Yoshihara teaches that by spinning a semiconductor wafer at high speeds, lowering the speed for a time, and re-increasing it to high speeds, the wafer can be coated with material in such a way that circular ripples do not appear thereon.

Yoshihara does not, however, teach or suggest that re-increasing the rate of spinning of a substrate may be affected gradually. Rather, as indicated in the tables of columns 9 and 10 of Yoshihara, the acceleration and deceleration between different spinning speeds are affected very quickly—at least 10,000 rpm/s.

Claim 3, however, requires that a second material be spread by spinning a semiconductor device structure at a first speed, gradually decreasing the rate of spinning to a second speed, and *gradually increasing* the rate of spinning to a third speed.

Lu does not provide any specifics as to how the photoresist layer 114 thereof is applied.

Accordingly, it is respectfully submitted that neither Lu nor Yoshihara, taken either separately or together, teaches or suggests "gradually increasing a rate of . . . spinning," as recited in claim 3.

Lu et al. in View of Jenq

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu in view of Jenq (hereinafter "Jenq").

Claims 6 and 7 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 1, which is allowable.

Further, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Lu and Jenq in the manner that has been asserted. In particular, Lu is drawn to a method for lining the surfaces of a recess (capacitor opening 110) with a layer of rugged polysilicon 112 to form the bottom electrode of a storage capacitor, while the method of Jenq includes forming shallow trench isolation structures by filling shallow trenches with silicon dioxide. Jenq, col. 4, lines 8-14. Jenq lacks any specifics about how the structure is formed, let alone whether or not planarization processes are conducted to ensure that the shallow trench isolation structure has a substantially planar surface and is coplanar with the active surface of the semiconductor substrate in which it is formed.

Accordingly, it appears that any motivation to combine the teachings of Lu and Jenq in the manner that has been asserted could only have been improperly gleaned from the subject matter described in the above-referenced application.

Lu et al. in View of Hsieh

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu in view of U.S. Patent 6,228,711 to Hsieh (hereinafter "Hsieh").

Claims 8 and 9 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 1, which is allowable.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 3-9 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1-22 is allowable. An early notice of the allowability of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

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